THE UNIVERSITY OF TEXAS AT AUSTIN

Cockrell School of Engineering

FULL NAME: Vijay Janapa Reddi

TITLE: Assistant Professor

DEPARTMENT: Electrical and Computer Engineering

RESEARCH AREAS: Computer Architecture; Compilers; Runtime Systems.

EXPERTISE DOMAINS: Mobile Computing; High-Performance Systems; Web Technologies.

EDUCATION:

Harvard University	Computer Science	Ph.D.	2010
University of Colorado—Boulder	Electrical and Computer Engineering	M.S.	2006
Santa Clara University	Computer Engineering	B.S.	2003

CURRENT AND PREVIOUS ACADEMIC POSITIONS:

University of Texas at Austin	Assistant Professor	August 2011 – Present

OTHER PROFESSIONAL EXPERIENCE:

Intel	Consultant	June 2015 – Present
Advanced Micro Devices (AMD)	Consultant	February 2015 – Present
Intel	Consultant	June 2014 – August 2014
Advanced Micro Devices (AMD)	Senior Design Engineer	July 2010 – July 2011
Microsoft Research	Research Intern	March 2009 – June 2009
VMware	Research Intern	January 2007 – March 2009
Intel	Research Intern	April 2003 – December 2006

HONORS AND AWARDS:

- IEEE TCCA Young Computer Architect Award, *IEEE Computer Society*, 2016.
- Top Picks Honorable Mention in Computer Architecture, *IEEE Micro*, 2016.
- Gilbreth Lectureship Award, *National Academy of Engineering (NAE)*, 2016.
- Most Influential PLDI Paper Award, *ACM SIGPLAN*, 2015.
- Indo-American Frontiers of Engineering, *National Academy of Engineering (NAE)*, 2014.
- Intel Early Career Honor Award, *Intel*, 2013.
- Google Faculty Research Award, *Google*, 2012, 2013, 2015.
- Top Picks in Computer Architecture, *IEEE Micro*, 2011.
- Top Picks in Computer Architecture, *IEEE Micro*, 2010.
- Best Paper Award, *Intl. Symp. on High Performance Computer Architecture (HPCA)*, 2009.
- John A. and Elizabeth S. Armstrong Fellowship, *Harvard University*, 2008.
- Best Student Presentation, *Intl. Symp. on Code Generation and Optimization (CGO)*, 2007.
- Top Picks in Computer Architecture, *IEEE Micro*, 2006.
- Best Paper Award, *International Symposium on Microarchitecture (MICRO)*, 2005.
- Faculty Recognition for Technical Excellence, *Santa Clara University*, 2003.
- Outstanding Undergraduate (Honorable Mention), *Computing Research Association (CRA)*, 2003.

MEMBERSHIPS IN PROFESSIONAL AND HONORARY SOCIETIES:

Member: Institute of Electrical and Electronics Engineers (IEEE)
Member: Association for Computing Machinery (ACM)

UNIVERSITY COMMITTEE ASSIGNMENTS:

Departmental-	Member, Faculty Recruiting Committee	2015
	Member, Technology in Teaching	2014
	Member, Faculty Recruiting Committee	2013
	Graduate Student Admissions Committee	2011- Present

PROFESSIONAL SOCIETY AND MAJOR GOVERNMENTAL COMMITTEES:

- General Chair, Intl. Symp. on Code Generation and Optimization (CGO 2017)
- Finance Chair, Intl. Symp. on Code Generation and Optimization (CGO 2015)
- Program Committee,
    - Intl. Symp. on Computer Architecture (ISCA 2014)
    - High Performance Computer Architecture (HPCA 2012, 2014, 2015)
    - Microarchitecture (MICRO 2013,2014)
    - Principles and Practice of Parallel Computing (PPoPP 2013, 2015)
    - Code Generation and Optimization (CGO 2013, 2014)
    - Parallel Architectures and Compilation Techniques (PACT 2013)
    - Workload Characterization (IISWC 2012, 2013, 2016)
    - Parallel & Distributed Processing (IPDPS 2012)
    - Intl. Symp. on Performance Analysis of Systems and Software (ISPASS 2012)
- Program Chair, Intl. Symp. on Code Generation and Optimization (CGO 2014)
- Guest Editor,
    - IEEE Micro Special Issue on Reliability-Aware Microarchitecture Design (2013),
    - IEEE Micro Special Issue on Internet of Things (2016)

- Local Arrangements Chair,
  - Intl. Symp. on Performance Analysis of Systems and Software (ISPASS 2013)
  - Workshop on Silicon Errors in Logic - System Effects (SELSE 2015, 2016)
- Publications Chair, Intl. Symp. on Workload Characterization (IISWC 2013)
- Organizer
  - Tutorial on Tools for Mobile Computer Architecture (MobiTools 2016)
  - Tutorial on Simulation and Analysis Engine (ISCA 2016, ASPLOS 2016, HPCA 2016, ICS 2016, IISWC 2015, ISPASS 2015)
  - Workshop on Resilient Architectures (WRA 2013–2010)
- Steering Committee, Intl. Symp. on Code Generation and Optimization (CGO)

COMMUNITY ACTIVITIES:

- Hands-on Computer Science (HaCS) for Austin Independent School District (via UT Outreach), https://outreach.uteach.utexas.edu/csp

PUBLICATIONS:

Google Scholar link, https://scholar.google.com/citations?user=gy4UVGcAAAAJ&hl=en&oi=ao

Refereed Conference Proceedings (34 Papers)

C1. T. Moseley, A. Shye, **V. Janapa Reddi**, M. Iyer, D. Fay, J. Kihm, A. Settle, D. Grunwald, D. Connors. "Dynamic Run-time Architecture Techniques for Enabling Continuous Optimization," in *ACM International Conference on Computing Frontiers (CF)*, pp.211-220, May 2005. http://dx.doi.org/10.1145/1062261.1062296

C2. C. Luk, R. Cohn, R. Muth, H. Patil, A. Klauser, G. Lowney, S. Wallace, **V. Janapa Reddi**, K. Hazelwood. "Pin: Building Customized Program Analysis Tools with Dynamic Instrumentation," in *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, vol 40(6), pp.190-200, June, 2005. http://dx.doi.org/10.1145/1064978.1065034

C3. S. Figueira, **V. Janapa Reddi**. "Topology-Based Hypercube Structures for Global Communication in Heterogeneous Networks," in *Euro-Par*, pp.994-1004, September 2005. http://dx.doi.org/10.1007/11549468_109

C4. A. Shye, M. Iyer, **V. Janapa Reddi**, D. Connors. "Code Coverage Testing Using Hardware Performance Monitoring Support," in *IEEE International Symposium on Automated and Analysis-Driven Debugging (AADEBUG)*, pp.159-163, September 2005. http://dx.doi.org/10.1145/1085130.1085151

C5. Q. Wu, **V. Janapa Reddi**, Y. Wu, J. Lee, D. Connors, M. Martonosi, D. Clark. "A Dynamic Compilation Framework for Controlling Microprocessor Energy and Performance," in *IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp.12-282, November 2005. http://dx.doi.org/10.1109/micro.2005.7

C6. T. Moseley, A. Shye, **V. Janapa Reddi**, D. Grunwald, R. Peri. "Shadow Profiling: Hiding Instrumentation Costs with Parallelism," in *IEEE/ACM International Conference on Code Generation and Optimization (CGO)*, pp.198-208, March 2007. http://dx.doi.org/10.1109/cgo.2007.35

C7. **V. Janapa Reddi**, D. Connors, R. Cohn, M. Smith. "Persistent Code Caching: Exploiting Code Reuse Across Executions and Applications," in *IEEE/ACM International Conference on Code Generation and Optimization (CGO)*, pp.74-88, March 2007. http://dx.doi.org/10.1109/cgo.2007.29

C8. A. Shye, T. Mosely, **V. Janapa Reddi**, J. Bloomstedt, D. Connors. "Using Process-Level Redundancy to Exploit Multiple Cores for Transient Fault Tolerance," in *IEEE Dependable Systems and Networks (DSN)*, pp.297-306, June 2007. http://dx.doi.org/10.1109/dsn.2007.98

C9. **V. Janapa Reddi**, M. Gupta, G. Holloway, G. Wei, M. Smith, D. Brooks. "Voltage Emergency Prediction: Using Signatures to Reduce Operating Margins," *in IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, pp.18-29, February 2009. http://dx.doi.org/10.1109/hpca.2009.4798233

C10. M. Gupta, **V. Janapa Reddi**, G. Holloway, G. Wei, D. Brooks. "An Event-Guided Approach to Reducing Voltage Noise in Processors," in *IEEE Design Automation and Test in Europe*, pp.160-165, April 2009. http://dx.doi.org/10.1109/date.2009.5090651

C11. **V. Janapa Reddi**, M. Gupta, M. Smith, G. Wei, D. Brooks, S. Capmanoni. "Software-Assisted Hardware Reliability: Abstracting Circuit-level Challenges to the Software Stack," in *ACM/EDAC/IEEE Design Automation Conference (DAC)*, pp.788-793, July 2009. http://dx.doi.org/10.1145/1629911.1630114

C12. **V. Janapa Reddi**, B. Lee, T. Chilimbi, K. Vaid. "Web Search Using Mobile Cores: Quantifying and Mitigating the Price of Efficiency," in *ACM/IEEE International Symposium on Computer Architecture (ISCA)*, vol 38(3), pp.314-325, June 2010. http://dx.doi.org/10.1145/1816038.1816002

C13. **V. Janapa Reddi**, S. Kanev, W. Kim, S. Campanoni, M. Smith, G. Wei, D. Brooks. "Voltage-Guided Smoothing: Characterizing and Mitigating Voltage Noise in Production Processors via Software Thread Scheduling," in *IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp.77-88, December 2010. http://dx.doi.org/10.1109/micro.2010.35

C14. P. Bailis, **V. Janapa Reddi**, S. Gandhi, D. Brooks, M. Seltzer. "Dimetrodon: Processor-level Preventive Thermal Management via Idle Cycle Injection," in *ACM/EDAC/IEEE Design Automation Conference*, pp.89-94, June 2011. http://dx.doi.org/10.1145/2024724.2024745

C15. **V. Janapa Reddi** and D. Brooks. "Resilient Architectures via Collaborative Design: Maximizing Commodity Processor Performance in the Presence of Variations," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol 30(10), pp.1429-1445, October 2011. http://dx.doi.org/10.1109/tcad.2011.2163635

C16. S. Campanoni, T. Jones, G. Holloway, **V. Janapa Reddi**, G. Wei, D. Brooks. "HELIX: Automatic Parallelization of Irregular Programs for Chip Multiprocessing," in *IEEE/ACM International Symposium on Code Generation and Optimization (CGO)*, pp.84-93, March, 2012. http://dx.doi.org/10.1145/2259016.2259028

C17. **V. Janapa Reddi**, D. Pan, S. Nassif, K. Bowman. "Robust and Resilient Designs from the Bottom Up: Technology, CAD, Circuit, and System Issues," in *IEEE International Symposium on Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.7-16, Jan. 30 – Feb.2, 2012. http://dx.doi.org/10.1109/aspdac.2012.6165064

C18. Y. Zhu, **V. Janapa Reddi**. "High-Performance and Energy-Efficient Mobile Web Browsing on Big/Little Systems," in IEEE *International Symposium on High Performance Computer Architecture (HPCA)*, pp.13-24, February 2013. http://dx.doi.org/10.1109/hpca.2013.6522303

C19. J. Leng, T. Hetherington, A. ElTantawy, S. Gilani, N. Kim, T. Aamodt, **V. Janapa Reddi**. "GPUWattch: Enabling Energy Optimizations in GPGPUs," in ACM/*IEEE International Symposium on Computer Architecture (ISCA)*, vol 41(3), pp.487-498, June 2013. http://dx.doi.org/10.1145/2485922.2485964

C20. Y. Zhu, **V. Janapa Reddi**. "WebCore: Architectural Support for Interactive Mobile Web Browsing," in ACM/*IEEE International Symposium on Computer Architecture (ISCA)*, pp.541-552, June 2014. http://dx.doi.org/10.1109/isca.2014.6853239

C21. C. Zhou, X. Wang, W. Xu, Y. Zhu, **V. Janapa Reddi,** C. Kim. "Estimation of Instantaneous Frequency Fluctuation in a Fast DVFS Environment Using an Empirical BTI Stress-Relaxation

Model," *in IEEE International Symposium on International Reliability Physics Symposium (IRPS)*, pp.2D.2.1-2D.2.6, June 2014. http://dx.doi.org/10.1109/irps.2014.6860593

C22. J. Leng, Y. Zu, M. Rhu, M. Gupta, **V. Janapa Reddi**. "GPUVolt: Modeling and Characterizing Voltage Noise in GPU Architectures," in IEEE *International Symposium on Low Power Electronics and Design (ISLPED)*, pp.141-146, August 2014. http://dx.doi.org/10.1145/2627369.2627605

C23. J. Leng, Y. Zu, **V. Janapa Reddi**. "GPU Voltage Noise: Characterization and Hierarchical Smoothing of Spatial and Temporal Voltage Noise Interference in GPU Architectures," in IEEE *International Symposium on High Performance Computer Architecture (HPCA)*, pp.161-173, February 2015. http://dx.doi.org/10.1109/hpca.2015.7056030

C24. Y. Zhu, M. Halpern, **V. Janapa Reddi**. "Event-based Scheduling for Energy-Efficient Quality of Service (eQoS) in Mobile Web Applications," in IEEE *International Symposium on High Performance Computer Architecture (HPCA)*, pp.137-149 February 2015. http://dx.doi.org/10.1109/hpca.2015.7056028

C25. M. Halpern, Y. Zhu, R. Peri, **V. Janapa Reddi**. "Mosaic: Cross-Platform User-Interaction Record and Replay for the Fragmented Android Ecosystem," in *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pp.215-224, March 2015. http://dx.doi.org/10.1109/ispass.2015.7095807

C26. J. Leng, A. Buyuktosunoglu, R. Bertran, P. Bose, **V. Janapa Reddi**. "Safe Limits on Voltage Reduction Efficiency in GPUs: A Direct Measurement Approach," in *IEEE International Symposium on Microarchitecture (MICRO)*, pp.294-307, December 2015. http://dx.doi.org/10.1145/2830772.2830811

C27. Y. Zu, C. R. Lefurgy, J. Leng, M. Halpern, M. S. Floyd, **V. Janapa Reddi**. "Adaptive Guardband Scheduling to Improve System-level Efficiency of the POWER7+," in *IEEE International Symposium on Microarchitecture (MICRO)*, pp.308-321, December 2015. http://dx.doi.org/10.1145/2830772.2830824

C28. Y. Zhu, D. Richins, M. Halpern, **V. Janapa Reddi**. "Microarchitectural Implications of Event-driven Server-side Web Applications," in IEEE *International Symposium on Microarchitecture (MICRO)*, pp.762-774, December 2015. http://dx.doi.org/10.1145/2830772.2830792

C29. M. Halpern, Y. Zhu, **V. Janapa Reddi**. "Mobile CPU's Rise to Power: Quantifying the Impact of Generational Mobile CPU Design Trends on Performance, Energy, and User Satisfaction," in IEEE *International Symposium on High Performance Computer Architecture (HPCA)*, pp.64-76, March 2016. http://dx.doi.org/10.1109/hpca.2016.7446054

C30. Y. Zhu, **V. Janapa Reddi**. "GreenWeb: Language Extensions for Energy Efficient Mobile Web Computing," in *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pp.145-160, June 2016. http://dx.doi.org/10.1145/2908080.2908082

C31. Y. Liu, Z. Yu, L. Eeckhout, **V. Janapa Reddi**, Y. Luo, X. Wang, Z. Wang, C. Xu. "Barrier-Aware Warp Scheduling for Throughput Processors," in *ACM International Conference on Supercomputing (ICS)*, June 2016. http://dx.doi.org/10.1145/2925426.2926267

C32. N. Chachmon, D. Richins, R. Cohn, M. Christensson, W. Cui, **V. Janapa Reddi**. "Simulation and Analysis Engine for Scale-out Workloads," in *ACM International Conference on Supercomputing (ICS)*, June 2016. http://dx.doi.org/10.1145/2925426.2926293

C33. Y. Zu, W. Huang, I. Paul, **V. Janapa Reddi**. "Ti states: Processor Power Management in the Temperature Inversion Region," in IEEE *International Symposium on Microarchitecture (MICRO)*, October 2016. Accepted.

C34. M. Kazdagli, **V. Janapa Reddi**, M. Tiwari. "Quantifying and Improving the Efficiency of Hardware-based Mobile Malware Detectors," in IEEE *International Symposium on Microarchitecture (MICRO)*, October 2016. Accepted.

Refereed Journal Proceedings (8 Papers)

J1. Q. Wu, M. Martonosi, D. Clark, **V. Janapa Reddi**, D. Connors, Y. Wu, J. Lee, D. Brooks. "Dynamic-Compiler-Driven Control for Microprocessor Energy and Performance," in IEEE *Micro's Top Picks in Computer Architecture*, vol 26(1), pp.119-129, January 2006. http://dx.doi.org/10.1109/mm.2006.9

J2. A. Shye, J. Bloomstedt, T. Mosely, **V. Janapa Reddi**, D. Connors. "PLR: A Software Approach to Transient Fault Tolerance for Multicore Architectures," in IEEE *Transactions on Dependable and Secure Computing (TDSC)*, vol 6(2), pp.135-148, November 2008. http://dx.doi.org/10.1109/tdsc.2008.62

J3. **V. Janapa Reddi**, M. Gupta, M. Smith, G. Wei, D. Brooks, K. Hazelwood. "Eliminating Voltage Emergencies via Software-Guided Code Transformations," in *ACM Transactions on Architecture and Code Optimization (TACO)*, vol 7(2), pp.1-28, September 2010. http://dx.doi.org/10.1145/1839667.1839674

J4. **V. Janapa Reddi**, M. Gupta, G. Holloway, M. Smith. "Predicting Voltage Droops Using Recurring Program and Microarchitectural Event Activity," in IEEE *Micro's Top Picks in Computer Architecture*, vol 30(1), p.110, January 2010. http://dx.doi.org/10.1109/mm.2010.25

J5. **V. Janapa Reddi**, S. Kanev, W. Kim, S. Campanoni, M. Smith, G. Wei, D. Brooks. "Voltage Noise in Production Processors," in IEEE *Micro's Top Picks in Computer Architecture*, vol 31(1), pp.20-28, February 2011. http://dx.doi.org/10.1109/mm.2010.104

J6. **V. Janapa Reddi**, B. Lee, T. Chilimbi, K. Vaid. "Mobile Processors for Energy-Efficient Web Search," in *ACM Transactions on Computer Systems (TOCS)*, vol 29(3), art.9, August 2011. http://dx.doi.org/10.1145/2003690.2003693

J7. Y. Zhu, A. Srikanth, J. Leng, **V. Janapa Reddi**. "Exploiting Webpage Characteristics for Energy-Efficient Mobile Web Browsing," in IEEE *Computer Architecture Letters (CAL)*, pp.33-36, October 2012. http://dx.doi.org/10.1109/l-ca.2012.33

J8. Y. Zhu, M. Halpern, **V. Janapa Reddi**. "The Role of the CPU in Energy-Efficient Mobile Web Browsing," in IEEE *MICRO — Special issue on Mobile Systems,* vol. 35(1), pp. 26-33, January 2015. http://dx.doi.org/10.1109/mm.2015.8

Books and Manuscripts (1 Book)

B1. **V. Janapa Reddi** and M. Gupta. *Resilient Architecture Design for Voltage Variation,* Synthesis Lectures on Computer Architecture, Morgan & Claypool Publishers, vol 8(2), pp.1-138, June 2013. http://dx.doi.org/10.2200/s00486ed1v01y201303cac022

Workshops (10 Papers)

W1. **V. Janapa Reddi**, A. Settle, D. Connors, R. Cohn. "PIN: A Binary Instrumentation Tool in Computer Architecture Research and Education," in *International Workshop on Computer Architecture Education (WCAE)*. June 2004. http://dx.doi.org/10.1145/1275571.1275600

W2. A. Shye, M. Iyer, T. Mosely, D. Hodgdon, D. Fay, **V. Janapa Reddi**, D. Connors. "Analysis of Path Profiling Information Generated with Performance Monitoring Hardware," in *ACM SIGARCH Workshop on Interaction between Compilers and Computer Architecture (INTERACT)*, pp. 33-43, February 2005. http://dx.doi.org/10.1109/interact.2005.3

W3. **V. Janapa Reddi**, D. Connors, R. Cohn. "Persistence in Dynamic Code Transformation Systems," in *ACM SIGARCH Workshop on Binary Instrumentation and Applications (WBIA)*, vol 33(5), pp. 69-74, December 2005. http://dx.doi.org/10.1145/1127577.1127591

W4. A. Shye, **V. Janapa Reddi**, T. Moseley, D. Connors. "Transient Fault Tolerance via Dynamic Process Redundancy," in *ACM SIGARCH Workshop on Binary Instrumentation and Applications (WBIA)*. October 2006.

W5. **V. Janapa Reddi**, M. Gupta, K. Rangan, S. Campanoni, G. Holloway, M. D. Smith, G. Wei, D. Brooks. "Voltage Noise: Why It's Bad, and What to Do About It," in *IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE)*. March 2009.
W6. S. Kanev, T. M. Jones, G. Wei, D. Brooks, **V. Janapa Reddi**. "Measuring Code Optimization Impact on Voltage Noise," in *IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE)*. March 2013.
W7. L. Guckert, M. O' Connor, S. Kumar Ravindranath, Z. Zhao, **V. Janapa Reddi**. "A Case for Persistent Caching of Compiled JavaScript Code in Mobile Web Browsers," in *Workshop on Architectural and Microarchitectural Support for Binary Translation*. March 2013.
W8. J. Leng, Y. Zu, **V. Janapa Reddi**. "Energy Efficiency Benefits of Reducing the Voltage Guardband on the Kepler GPU Architecture," in *IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE)*. March 2014.
W9. S. Chai, D. Zhang, J. Leng, **V. Janapa Reddi**. "Lightweight Detection and Recovery Mechanisms to Extend Algorithm Resiliency in Noisy Computation," in *Workshop on Nearthreshold Computing* (co-located with ISCA), June 2014.
W10. M. Kazdagli, L. Huang, **V. Janapa Reddi**, M. Tiwari. "Morpheus: Benchmarking Computational Diversity in Mobile Malware," in Workshop on Hardware and Architectural Support for Security and Privacy. June 2014. http://dx.doi.org/10.1145/2611765.2611767

Technical Reports (1 Paper)

R1. **V. Janapa Reddi**, B. Lee, T. Chilimbi, K. Vaid. "Web Search Using Small Cores: Quantifying the Price of Efficiency," in Microsoft Research Tech. Report, June 2010.

Theses (3 Papers)

Th1. **V. Janapa Reddi**. "Heterogeneous Networks of Workstations Across Wide Area Networks," B.S. Thesis, Department of Electrical and Computer Engineering, Santa Clara University. June 2003.
Th2. **V. Janapa Reddi**. "Deploying Dynamic Code Transformation in Modern Computing Environments," M.S. Thesis, Department of Electrical and Computer Engineering, University of Colorado. November 2005.
Th3. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability: Enabling Aggressive Timing Speculation Using Run-Time Feedback from Hardware and Software," Ph.D. Thesis, School of Engineering and Applied Sciences, Harvard University. March 2010.

ORAL PRESENTATIONS:

Invited Talks and Seminars

O1. **V. Janapa Reddi**. "Persistent Code Caching," Intel, Santa Clara–CA, March 2007.
O2. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," Intel, Santa Clara–CA, March 2010.
O3. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," AMD, Austin–TX, March 2010.
O4. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," Microsoft Research, Redmond–WA, June 2010.
O5. **V. Janapa Reddi**. "Web Search Using Small Cores," Amazon, Seattle–WA, June 2010.
O6. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," Intel, Portland–OR, July 2010.
O7. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," IBM T. J. Watson Labs, Yorktown–NY, July 2010.
O8. **V. Janapa Reddi**. "Web Search Using Small Cores," SeaMicro, Santa Clara–CA, July 2010.
O9. **V. Janapa Reddi**. "Web Search Using Small Cores," Google, Palo Alto–CA, July 2010.
O10. **V. Janapa Reddi**. "Web Search Using Small Cores," HP Labs, Palo Alto–CA, July 2010.

O11. **V. Janapa Reddi**. "Web Search Using Small Cores," Facebook, Palo Alto–CA, July 2010.
O12. **V. Janapa Reddi**. "Web Search Using Small Cores," IBM T. J. Watson Labs, Hawthorne–NY, July 2010.
O13. **V. Janapa Reddi**. "Web Search Using Small Cores," Intel, Hudson–MA, July 2010.
O14. **V. Janapa Reddi**. "Web Search Using Small Cores," AMD, Boxborough–MA, October 2010.
O15. **V. Janapa Reddi**. "Toward High-Performance and Energy-Efficient Mobile Web Browsing," Intel, Austin–TX, August 2012.
O16. **V. Janapa Reddi**. "Toward High-Performance and Energy-Efficient Mobile Web Browsing," *AMD*, Austin–TX, August 2012.
O17. **V. Janapa Reddi**. "Toward High-Performance and Energy-Efficient Mobile Web Browsing," Qualcomm, Santa Clara–MA, February 2013.
O18. **V. Janapa Reddi**. "Architectural Support for the Interactive Mobile Web," Intel, Austin–TX, February 2014.
O19. **V. Janapa Reddi**. "Robust and Resilient Systems from the Bottom-Up: Circuits, Architecture and Software Integration," ISSCC Forum, San Francisco–CA, February 2014.
O20. **V. Janapa Reddi**. "Architectural Support for the Interactive Mobile Web," Samsung, Austin–TX, March 2014.
O21. **V. Janapa Reddi**. "Architectural Support for the Interactive Mobile Web," *ARM*, Austin–TX, March 2014.
O22. **V. Janapa Reddi**. "Mobile Processor Architectures: Design Implications and Challenges for Energy Efficiency," Indo-American Frontiers of Engineering (IAFOE), Mysore–India, May 2014.
O23. **V. Janapa Reddi**. "Hardware and Software Co-Design for Robust and Resilient Execution," International Conference on Integrated Circuit Design and Technology (ICICDT), Austin–TX, May 2014.
O24. **V. Janapa Reddi**. "Architecting for the Mobile Web: Where We've Been, Where We're Heading, and What We Need to Address," Parallelism in Mobile Platforms (PRISM) held in conjunction with International Symposium on Computer Architecture, June 2014.
O25. **V. Janapa Reddi**. "Simulators are Perfect, Authors are Oracles, Users are Innocent," Workshop on Duplicating, Deconstructing and Debunking (WDDD) held in conjunction with International Symposium on Computer Architecture, June 2014.
O26. **V. Janapa Reddi**. "Watt-Wise Web: Architecting for a Responsive and Energy-Efficient Mobile Web," Univ. of Michigan, November 2014.
O27. **V. Janapa Reddi**. "Mobile CPU Evolution: The Past, the Present, and the Future," Intel, Santa Clara–CA, February 2015.
O28. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," Facebook, Menlo Park–CA, March 2015.
O29. **V. Janapa Reddi**. "Mobile CPU Evolution: The Past, the Present, and the Future," Microsoft, Seattle–WA, April 2015.
O30. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," Qualcomm, Raleigh–NC, April 2015.
O31. **V. Janapa Reddi**. "Voltage Noise in Multicore Processors," Intel, Portland–OR, May 2015.
O32. **V. Janapa Reddi**, "GPU Voltage Guardband Management to Achieve Exascale Energy-Efficiency," Intel, Portland–OR, May 2015.
O33. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," Duke University, Raleigh–NC, June 2015.
O34. **V. Janapa Reddi**. "GPU Voltage Guardband Management to Achieve Exascale Energy-Efficiency," *AMD*, Austin–TX, June 2015.

O35. **V. Janapa Reddi**. "Mobile CPU Evolution: The Past, the Present, and the Future," Taiwan Application Processor Union – Mobile SoC Summer Course, Taiwan, September 2015.
O36. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," Mediatek, Taiwan, September 2015.
O37. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," National Taiwan University, Taiwan, September 2015.
O38. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," Academia Sinica, Taiwan, September 2015.
O39. **V. Janapa Reddi**. "Watt-Wise Web: Architecting for a Responsive and Energy-Efficient Mobile Web," Georgia Tech University, October 2015.
O40. **V. Janapa Reddi**. "Watt-Wise Web: Architecting for a Responsive and Energy-Efficient Mobile Web," Google Faculty Summit, October 2015.
O41. **V. Janapa Reddi**. "Watt-Wise Web: Architecting for a Responsive and Energy-Efficient Mobile Web," Texas A&M University, November 2015.
O42. **V. Janapa Reddi**. "Programming the Web of Things," Workshop on Internet of Things (IoT) held in conjunction with International Symposium on Microarchitecture, Hawaii, December 2015.
O43. **V. Janapa Reddi**. "End of the Road for My CAREER," Workshop on Negative Outcomes, Post-mortems, and Experiences (NOPE) held in conjunction with International Symposium on Microarchitecture, Hawaii, December 2015.
O44. **V. Janapa Reddi**. "From Moore's Law to Moore's Crawl: Architecting the Next-Generation of Mobile Computing Devices," University of Washington, Seattle–WA, February 2016.
O45. **V. Janapa Reddi**. "From Moore's Law to Moore's Crawl: Architecting the Next-Generation of Mobile Computing Devices," National Academy of Engineering (NAE) Annual Event, Irvine–CA, February 2016.
O46. **V. Janapa Reddi**. "Mobile CPU Evolution: The Past, the Present, and the Future," Rice University – TexasWISE Keynote, Houston, May 2016.
O47. **V. Janapa Reddi**. "Microarchitectural Implications of Event-driven Programming," Intel, Santa Clara–CA, May 2016.
O48. **V. Janapa Reddi**. "Microarchitectural Implications of Event-driven Programming," AMD, Austin–TX, May 2016.
O49. **V. Janapa Reddi**. "Microarchitectural Implications of Event-driven Programming," Northwestern, Chicago–IL, May 2016.
O50. **V. Janapa Reddi**. "Watt-WiseWeb://Architecting for Responsiveness and Energy-Efficiency," The University of Chicago, Chicago–IL, May 2016.

Other Major Presentations

T1. R. Cohn and **V. Janapa Reddi**. "Software Instrumentation and Hardware Profiling for Intel Itanium Linux," International Symposium on Code Generation and Optimization (CGO), 2004.
T2. C. Luk, D. Connors, W. Hsu, T. Moseley, **V. Janapa Reddi**. "Software Instrumentation as a Tool for Architecture and Compiler Research," International Symposium on Architectural Support for Programming Languages and Operating (ASPLOS), 2004.
T3. K. Hazelwood and **V. Janapa Reddi**. "Using Pin for Compiler and Computer Architecture Research and Education," International Symposium on Programming Language Design and Implementation (PLDI), 2007.

T4. K. Hazelwood, **V. Janapa Reddi**, D. Kaeli, D. Connors. "Hands-on Pin! for Architecture, OS and Program Analysis Research," International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2007.
T5. S. Campanoni and **V. Janapa Reddi**. "ILDJIT Compiler Framework for Architecture Research," International Symposium on Microarchitecture (MICRO), 2010.
T6. **V. Janapa Reddi.** "Hardware and Software Co-design for Robust and Resilient Execution," International Conference on IC Design and Technology (ICICDT), 2012.
T7. N. Chachmon, M. Christensson, R. Cohn, **V. Janapa Reddi.** "SIMICS 2015: System-level Program Analysis and Architectural Evaluation with Simics," International Symposium on Performance Analysis of Systems and Software (ISPASS), 2015.
T8. N. Chachmon, M. Christensson, R. Cohn, **V. Janapa Reddi.** "SIMICS 2015: System-level Program Analysis and Architectural Evaluation with Simics," International Symposium on Workload Characterization (IISWC), 2015.
T9. N. Chachmon, M. Christensson, **V. Janapa Reddi.** "Intel SAE: A Dynamic Binary Instrumentation Framework for Full-System Simulation and Analysis," International Symposium on High Performance Computer Architecture (HPCA,), 2016.
T10. N. Chachmon, D. Richins, M. Christensson, **V. Janapa Reddi.** "Intel SAE: A Dynamic Binary Instrumentation Framework for Full-System Simulation and Analysis," International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2016.
T11. N. Chachmon, D. Richins, M. Christensson, **V. Janapa Reddi.** "Intel SAE: A Dynamic Binary Instrumentation Framework for Full-System Simulation and Analysis," International Conference on Supercomputing (ICS), 2016.
T12. N. Chachmon, D. Richins, M. Christensson, **V. Janapa Reddi.** "Intel SAE: A Dynamic Binary Instrumentation Framework for Full-System Simulation and Analysis," International Symposium on Computer Architecture (ISCA), 2016.
T13. Y. Zhu, M. Halpern, **V. Janapa Reddi.** "MobiTools: Tutorial on Infrastructure and Tools for Mobile Computer Architecture Research with an Emphasis on Real System Measurement," International Symposium on Computer Architecture (ISCA), 2016.
T14. D. Richins, B. Gowda, N. Chachmon, M. Christensson, **V. Janapa Reddi.** "BigBench+SAE: Instrumenting an Industry-strength BigData Benchmark for BigData Analytics," International Symposium on Microarchitecture (MICRO), 2016.

PATENTS:

P1. R. Cohn, T. Moseley, and **V. Janapa Reddi**. "System and method to instrument references to shared memory." U.S. Patent Application 11/143,130, filed June 1, 2005.
P2. N. Kim, J. O'Connor, M. Schulte, and **V. Janapa Reddi**. "Method and apparatus for power reduction during lane divergence." U.S. Patent Application 13/605,460, filed September 6, 2012.
P3. **V. Janapa Reddi**, M. Gupta, G. Holloway, G. Wei, M. D. Smith, and D. Brooks. "Adaptive event-guided system and method for avoiding voltage emergencies." U.S. Patent 8,949,666, issued February 3, 2015.

GRANTS, CONTRACTS and GIFTS:

Grants and Contracts

PI/Co-PI	Title	Agency	Grant Period	Total/ My Share

PI Janapa Reddi (self)	High-Performance, Energy-Efficient Mobile Web Computing	National Science Foundation	06/01/2016 - 05/31/2019	$400,000/ $400,000
PI Chris Kim (Univ. of Minnesota)/ Co-PI Janapa Reddi	Second Phase of Circuit and Architecture Co-Design for Near Threshold Voltage-Based Mobile Application Processors	Univ. of Minnesota (subcontract)	04/10/2015 - 01/10/2016	$100,000/ $43,500
PI Janapa Reddi/ Co-PI Chris Kim (Univ. of Minnesota)	Feedback-Driven Resiliency for Near-Threshold Systems: under SRC MAG (201300745-001;2013-HJ-2408 MAG)	Semiconductor Research Corporation	04/01/2013 - 03/31/2017	$128,000/ $64,000
PI Chris Kim (Univ. of Minnesota)/ Co-PI Janapa Reddi	Circuit and Architecture Co-Design for Near Threshold Voltage-Based Mobile Application Processors	Univ. of Minnesota (subcontract)	12/15/2013 - 01/15/2015	$100,000/ $43,500
PI Janapa Reddi/ Co-PI Sek Chai (SRI)	Resilient Computing Systems Using Deep Learning Techniques	National Science Foundation	08/01/2015 - 07/31/2018	$499,959/ $265,000
PI Janapa Reddi/ Co-PI Chris Kim (Univ. of Minnesota)	Feedback-driven resiliency for Near Threshold Systems	National Science Foundation	04/01/2013 - 03/31/2016	$192,000/ $96,000
PI Janapa Reddi/ Co-PI Lizy John (UT Austin)	Cross-Layer Solutions for Sustainable and Reliable Computing Solutions	National Science Foundation	08/01/2012 - 07/31/2015	$300,000/ $214,670

Industry Gifts

PI/Co-PI	**Title**	**Agency**	**Grant Period**	**Grant Total**
PI Janapa Reddi (self)	Mobile computing	Google	2012, 2013, 2015	$139,000
PI Janapa Reddi (self)	Reliability and Mobile Computing	Intel	2012, 2013, 2015, 2016	$395,000
PI Janapa Reddi (self)	Power modeling	AMD	2012, 2013, 2014, 2015	$150,000
Total Funding:				**$2,403,959**
My Total Funding:				**$1,810,670**

PH.D. STUDENTS:

A. Students defended
    a. Jingwen Leng (passed, expected graduation December 2016)

B. Students in candidacy, passed Ph.D. qualifying exam
    a. Yuhao Zhu

C. Post M.S. students, preparing to take Ph.D. qualifying exam
    a. Richins, Daniel
    b. Halpern, Matthew

D. Pre M.S. students, passed Ph.D. pre-qualifying exam
    a. Zhu, Yazhou
    b. Cui, Wenzhi

M.S. STUDENTS:

A. Students graduated:
    a. Srikanth, Aditya (May 2013)
    b. Garg, Ankita (co-supervised, May 2013)

BRIEF VITA:

Vijay Janapa Reddi is an Assistant Professor in the Department of Electrical and Computer Engineering at the University of Texas at Austin. His research interests span the definition of computer architecture, including software design and optimization, to enhance mobile quality-of-experience and improve the energy-efficiency of high-performance computing systems. Dr. Janapa Reddi is a recipient of the National Academy of Engineering Gilbreth Lectureship honor (2016), IEEE Computer Society TCCA Young Computer Architect Award (2016), Intel Early Career Award (2013) and multiple Google Faculty Research Awards (2012, 2013, 2015). He is also the recipient of the Best Paper at the 2005 International Symposium on Microarchitecture, Best Paper at the 2009 International Symposium on High-Performance Computer Architecture, and IEEE's Top Picks in Computer Architecture awards (2006, 2010, 2011). Beyond his scientific research contributions, Dr. Janapa Reddi is passionate about starting STEM education at an early age. He is responsible for the Austin Independent School District's "hands-on" computer science (HaCS) program, which teaches 5th and 6th-grade students programming and the principles that govern a modern computing system using Arduino devices. He received a BS in computer engineering from Santa Clara University, an MS in electrical and computer engineering from the University of Colorado at Boulder, and a Ph.D. in computer science from Harvard University.